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CAN THE METALS REPLACE SEMICONDUCTORS IN A NOTHING ON INSULATOR NANOTRANSISTOR ?

Cristian RAVARIU[1], Avireni SRINIVASULU[2], Dan E. MIHAIESCU[1], Elena MANEA[3], Cătălin PARVULESCU[3]

[1] Politehnica University of Bucharest, Splaiul Independentei 313, Sector 6, 060042, Bucharest, Romania
[2] JECRC University, Dept. of ECE, Jaipur – 303905, Rajasthan State, India
[3] National Institute for Research and Development in Microtechnologies – IMT Bucharest,
Street Erou Iancu Nicolae 126A, 077190, Voluntari, Ilfov, Romania

Corresponding author: Cristian RAVARIU, E-mail: cristian.ravariu@upb.ro

Abstract. The CMOS technology will reach very soon its physical limit. In the next decade, the CMOS success will continue by co-integration with other nanodevices, accordingly to the Electron Device Society estimations. The vacuum nano-transistors represent a promising solution. The Nothing On Insulator transistor belongs to these devices class of international interest. The paper has the goal to establish if metals can replace semiconductors for the Nothing On Insulator (NOI) devices. The work is based on simulations and comparisons with other similar fabricated devices that cited our previous work. Due to the well-known electrons emission from metals in vacuum it is expected to efficiently replace the semiconductors by metals. The deposition of tens nanometer of metal as source/drain islands onto a thin oxide would be a simpler and cheaper technology to fabricate NOI nano-devices. The actual analysis is based on an extremely precise model, available as quantum tunneling through the Metal-Insulator-Metal (MIM) ultra-thin structures, activated by MIMTUN function in simulator and measured in MIM structures by other authors. The I_D-V_{DS} characteristics allow the NOI device with metals to generate pure exponential functions in some applications. The second class of characteristics, I_D-V_{GS} seem to offer a constant slope and a poor gate modulation. But this constant slope is an excellent hint to provide constant resistances at given V_{GS}, ranging from 5kohm to 5Gohm, for a resistor size of tens nanometer. This is excellent for the CMOS transistors co-integration with so tiny resistors in nanoscale electronics.

Key words*:* future CMOS, nanoscale, vacuum device physics, metal-insulator-metal, tunneling.

1. INTRODUCTION

The CMOS integrated circuits miniaturization allows a large variety of new nano-scale devices to be proposed as possible competitors to CMOS, like quantum devices [1], Tunnel-FETs [2], nanowire-FETs [3]. Within the last integrated circuits [4], it is hard to believe that CMOS fails in front of any alternative competitor. Therefore, alternative solutions come with co-integration concepts [5], taking care of the Si-technology compatibility, filling the CMOS gaps [6]. In 2014, a NASA research team fabricated a vacuum nanotransistor that seems to reply to the ultimate demands of the vacuum tubes [7], transistoring the vacuum tubes, making them able for co-integration and covering the tera-hertz gap, a frequency interval from 30GHz to 30THz, where the semiconductor devices fail [6].

In recent years, a SOI related device with a vacuum nano-cavity, also called the NOI (Nothing On Insulator) transistor [8-13], use similar tunneling conduction and joins to this vacuum nanotransistor class of international interest [6, 14]. The NOI implementation in Silicon is difficult, particularly for the growing of the source and drain islands, as two Silicon On Insulator mono-crystalline films of 10-20nm thickness at 2-5nm distance [10]. To deposit two metallic layers, as source/drain islands of 10-20nm onto a thin oxide of 10-20nm, grown on a Si-wafer, is simpler and cheaper. The sole challenge rests the nano-cavity configuration. This NOI device variant with the succession Metal/Vacuum as Insulator/Metal on insulator is abbreviated as NOI-MIM device, in this paper. Before the technological fabrication, the question is: can metal replace semiconductor source/drain islands? Usually metals emit electrons in vacuum so that, the source-drain conduction at a given drain voltage is expectable [15].

Very recent, some researcher tried to fabricate a vacuum MIM conduction by 35nm of air [16], citing our previous work, too. The scope begin to be defined: a nano-scale, metal-based field emission air channel transistors fabrication [16, 17]. Such downscaling allows cold cathode emission, where only the electric field is strong enough to permit current flow. Operating voltages can be reduced to less than 10V [17] and this become promising for the perspective of the CMOS co-integration.

Some hypothesis have to be clarified: (i) what tunneling mechanism is suitable in the device simulator to model the NOI-MIM conduction; (ii) if the I_D-V_{DS} curves keep the same exponential dependence as NOI transistor in Si [11, 12]; (iii) if the I_D-V_{GS} curves keep two ON/OFF distinct states, at least in weak tunneling regime [13]; (iv) comparison of the simulation results with appropriate real measurements [16-19]; (v) applications of the NOI-MIM. The paper is structured on the following sections: (1) Introduction; (2) Presentation of the NOI-MIM structure and convenient simulation models, (3.1) Transfer characteristics simulation; (3.2) Output characteristics simulation; (4) Discussions of some phenomena and comparisons with related devices and (5) Conclusions.

2. THE NOI-MIM STRUCTURE AND MODELS

The NOI-MIM structure is simulated by Atlas from Silvaco as simulator, selecting similar size as NOI in Si [10-12], keeping the size as small as possible (Fig. 1). The Si-wafer under oxide is not represented, as in usual SOI simulations. The drain and source islands consist of conductors of 10nm thickness, placed on SiO_2 layer of 10nm. For the sake of proportionality on horizontal axis, the source and drain length is 4nm, while the cavity length is 2nm. In reality, the source and drain can be longer, which is less important in simulations.

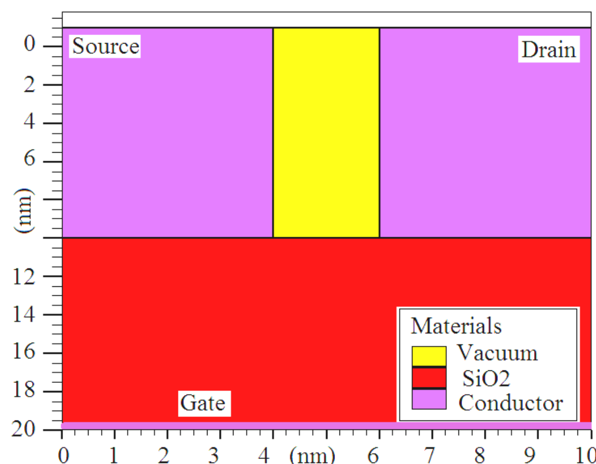

Fig. 1 – The NOI variant with MIM-Metal-Vacuum-Metal succession and the Gate as bottom contact.

In a first step, the proper tunneling model is established. In this scope, we start from a previous study that proved a Fowler-Nordheim (FNORD) tunneling model in conjunction with SIS (Semiconductor-Insulator-Semiconductor) parameter activation for a proper simulation of a NOI in Si [11]. Now, the NOI-MIM device with two conductors separated by 2nm of insulator, can be also dominated by a quantum tunneling (QTUNN) through this nano-cavity. The QTUNN model was tested for NOI in Si too, but with minor relevance [11]. In Atlas, in order to capture the quantum tunneling current through the succession Metal-Insulator-Metal (MIM), a dedicated function must be activated: MIMTUN. In this way, the band structure values are interpolated onto the tunneling paths, solving the Schrodinger equation and computing the transmission probability of electrons through the potential barrier of the ultrathin insulator [20].

In order to select the proper tunneling model for the NOI-MIM device, the I_D-V_{DS} curves are simulated at V_{GS}=+2V by different models: Fowler-Nordheim (FNORD), quantum tunneling model (MIMTUN), Zaidman model (ZAID) and all are compared to the most successful model for the NOI variant in Si that is (FNORD+SIS) model [11] (Fig. 2). For the NOI-Si simulation, the size of this structure exactly copies the size

of NOI-MIM from Fig. 1, plus the additional features of the semiconductor islands as in reference [11]. The results show that the main current component through NOI-MIM is given by the MIMTUN model, being comparable with the current through the NOI-Si variant. Zaidman model is sometimes suitable for the vacuum triodes simulations [21], being a FNORD model plus a linear acceleration of the injected electrons in vacuum.

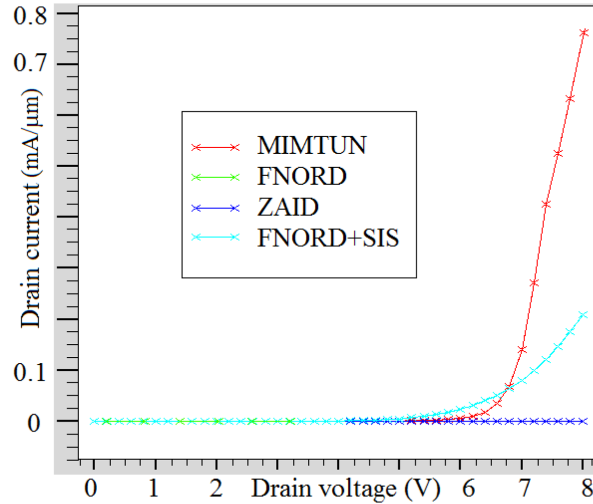

Fig. 2 – The I_D-V_{DS} simulated curves at $V_{GS}=+2$V at linear scale.

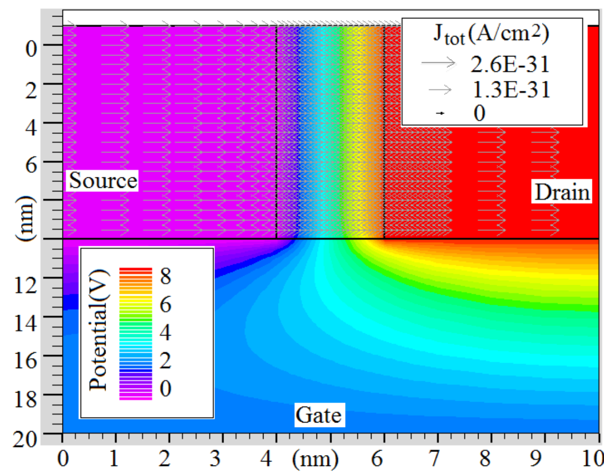

Fig. 3 – The simulated current vectors flowing through the biased NOI-MIM device.

The carrier acceleration is poor inside a vacuum cavity of 2nm. So, any Fowler-Nordheim current is minor in the NOI-MIM case. In conclusion, the most suitable model is the quantum tunneling, described by MIMTUN parameter, for the conduction through the NOI-MIM device.

A functional simulation shows the potential distribution, as colored contours and conduction current vectors through the NOI-MIM device, biased at $V_S=0$V, $V_D=8$V, $V_G=2$V (Fig. 3).

3. THE NOI-MIM CHARACTERISTICS

3.1. The output characteristics

At this stage, a non-linear I_D-V_{DS} dependence is expected. The NOI-MIM device with MIMTUN model is simulated at $V_S=0$V, ranging the drain voltage between 0V to 8V, keeping by turn a constant gate voltage: $V_G=-3$V, 0.8V, 2V, 4V, 7V (Fig. 4a,b).

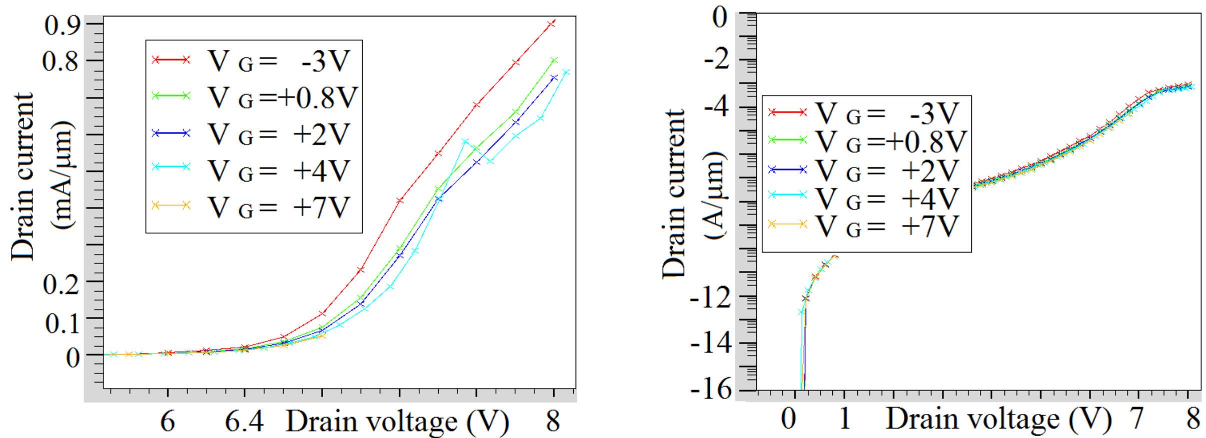

Fig. 4 – The simulated I_D-V_{DS} curves for the NOI-MIM structure at: (a) linear scale – detail, (b) log scale.

The simulations reveal a strong non-linear characteristic, exponential-like function. At V_{DS}=8V the current is 0.8mA for NOI-MIM at V_{GS}=–3V, 0.7mA for NOI-MIM at V_{GS}=+7V and 0.24mA for NOI-Si at V_{GS}=+2V (Fig. 4a). However, the logarithmic scale shows a constant slope for the logI_D-V_{DS} curves of a NOI device with metals (Fig. 4b). This means the NOI-MIM variant generates a clear exponential function on a large V_{DS} range, like a bipolar transistor or a pn diode. Obviously, the gate voltage has almost null influence on the drain current (Fig. 4b) versus the NOI-Si case [11].

3.2. The transfer characteristics

The simulated I_D-V_{GS} curves are presented in Fig. 5. In this scope, the NOI-MIM device with MIMTUN model is biased at V_S=0V, ranging the gate voltage between –10V to 10V, keeping by turn a constant drain voltage: V_D=0.8V, 1V, 2V, 5V, 8V. For a NOI with Si-films, the gate voltage ranging from negative to positive values brings the Si-islands from accumulation to inversion and allows different current emission in vacuum [13]. This phenomenon is absent in metals. Hence, we assist to a poor variation of the drain current with the gate voltage for NOI-MIM devices (Fig. 5).

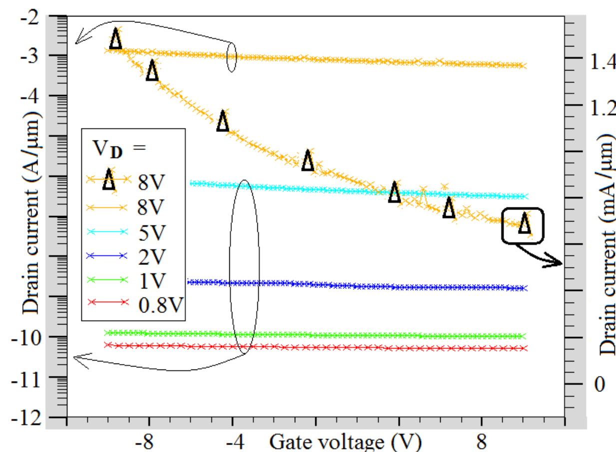

Fig. 5 – A family of the I_D-V_{GS} curves of a NOI-MIM structure – at the left side and a curve at V_D=8V at linear scale – right side.

Neither the strong (V_D=8V) or weak (V_D=0.8V) tunneling regime [12], stimulate the transition from an ON to an OFF state. The condition of the drain current modulation under a gate voltage – specific to a field effect transistor – is not fulfilled. This quasi-linear transfer characteristic is the main reason for the invalidation of the NOI-MIM structure as tunnel field effect transistor.

From Fig. 5, a secondary application results for a NOI-MIM device - a resistor commanded by the gate voltage. The drain-source average resistance is: 10kΩ at V_{DS}=8V, 10MΩ at V_{DS}=5V or 5GΩ at V_{DS}=2V.

4. DISCUSSIONS AND COMPARISONS

For a final invalidation of the NOI-MIM structure as transistor, its transfer characteristic is compared to the characteristics of the other NOI variants in Si from previous references [10, 11] and PIN [22] in the most sensitive regime – the weak tunneling, at V_{DS}=0.8V (Fig. 6). The same geometry can be compared to: NOI-Si1 and NOI-MIM structures with 15nm×26nm oxide, 10nm×2nm islands and flat cavity. The variant in Silicon – NOI-Si2 additional gets nano-rectangular grains as roughnesses of the cavity walls, while the NOI-Si3 in Si has thinner oxide of 10nm. The PIN-sim is a structure of PIN Tunnel-FET with doping from reference [22], identical size as NOI-MIM, while the PIN-exper reflects some I_D-V_{GS} picked points from measured PIN-Tunnel-FET [22]. Because, chronologically speaking, the first vacuum nano-transistor with semiconductor islands was fabricated in 2012 [18], its characteristics are included, too in Fig. 6.

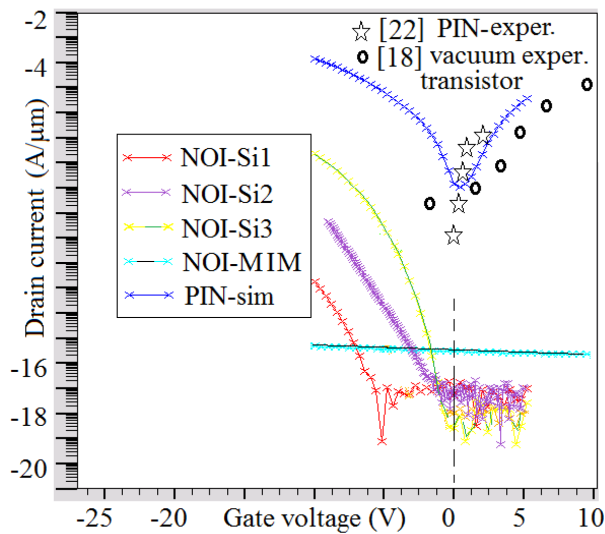

Fig. 6 – The I_D-V_{GS} curves comparatively presented for different tunnel devices.

Rather, the NOI characteristics must be compared to the experimental values of the most related device – a vacuum nanotransistor with a tunneling through a vacuum cavity, using I_D-V_{GS} picked points [18]. The predicted hypothesis regarding the NOI-MIM structure is fulfilled in Fig. 6, offering a quasi-constant current, I_D-V_{GS}. However, the fabricated vacuum transistor from reference [18] benefits on larger size, especially on Oz axis, where the Atlas simulations admits by default 1μm device depth. So, the currents are systematically higher.

Much more concluding are the comparisons of the simulated NOI-MIM actual variants with similar experimental devices. In Fig. 7 the output characteristic I_D-V_{DS} of a NOI-MIM device is compared to similar characteristics of other devices: NOI-Si1, NOI-Si3 (simulated), a metal-air transistor fabricated in 2018 [16] (experimental) and a pure MIM tunneling device [19] (experimental).

The I_D-V_{DS} comparison reveals the same level of current for NOI-MIM device with metal and NOI-Si1,2 with Silicon and vacuum transistors [20]. The tunnel current through two metals separated by 10nm insulator of a MIM device was converted from the current density given in [19], considering area of 1cm^2. A significant clue is the constant slope of the log I_D-V_{DS} curve. The NOI-MIM structure, vacuum transistor or MIM device gets quite similar slopes that means an accurate exponential function I_D-V_{DS}. This comparison proves the potential applications of the NOI-MIM device as a nano-diode using the I_D-V_{DS} exponential curves, or as a MIM tunneling device that is used in full-color display panels [19]. The closest variant of Metal-Air nanotransistor fabricated in 2018 [16] confirms the simulation results about the I_D-V_{DS} shape and

also indicates vacuum nanodevices working at low voltages around 1V, see [16] and Fig. 7. In multiple applications, these NOI-MIM features can be used [23–26].

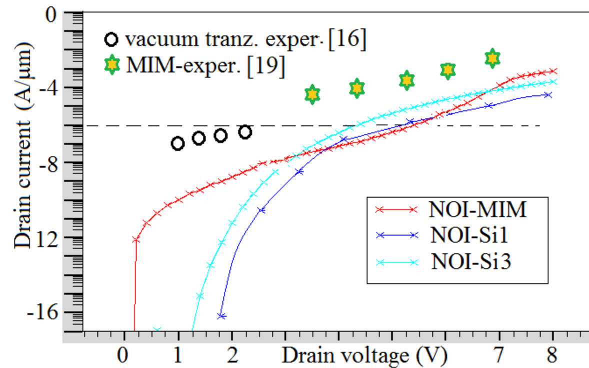

Fig. 7 – The I_D-V_{DS} curves comparatively presented for different tunnel devices.

5. CONCLUSIONS

To the question – can the metal replace semiconductors – the simulations gave the following answers:

– NOI-MIM devices lose the gate control on the source-drain current, because in metals do not occur the phenomena of accumulation, depletion or inversion as in semiconductors. But the NOI-MIM variants with metals present constant slope of the transfer characteristics, I_D−V_{GS}. This feature offers a large spectrum for the source-drain resistance at a given V_{DS} – 5kΩ –5GΩ, controlled by a given V_{DS}. Hence, the NOI-MIM variant will be an excellent solution for a nano-size integrated resistor.

– NOI-MIM devices obey to the exponential I_D−V_{DS} law. So that, NOI-MIM device is working well as a MIM tunneling device, being able to generate exponential function as I_D−V_{DS} dependence, replacing diodes of large aria.

In conclusion, if the source/drain regions are semiconductors, the NOI device with this source-drain configuration works as transistor. If the source/drain islands are metals, the NOI device can be an exponential generator or a controlled resistor. It can be applied as a diode using its I_D−V_D characteristics, or as a resistor with an electrical resistance ranging from kilo to giga-ohms. In all these cases, the applications of NOI-MIM devices, either as resistors or diodes, consuming an area per chip from 10×10 nm^2 up to 100×100 nm^2, make from these NOI-MIM devices excellent candidates for next co-integration with ULSI CMOS circuits.

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